WHAT IS CLAIMED IS:

1. A method for providing a data path through a Small Form Factor Pluggable (SFP) transceiver, the SFP transceiver being substantially interfaced with a host device, the SFP transceiver including a plurality of single-ended pins, the method comprising:

determining if the SFP transceiver is suitable for use in supporting lower speed applications;

using the plurality of single-ended pins to provide at least one of a TX CLOCK signal, a TX DATA signal, an RX CLOCK signal, and an RX DATA signal when it is determined that the SFP transceiver is being used for the lower speed application.

2. The method of claim 1 further including:

using the plurality of single-ended pins to provide at least one control signal and at least one status signal when it is determined that the SFP transceiver is not being used for the lower speed application.

3. The method of claim 2 wherein when it is determined that the SFP transceiver is not being used for the lower speed application, the SFP transceiver is being used for a higher speed application.

4. The method of claim 3 wherein the higher speed application is one of a Fiber Channel application, a Gigabit Ethernet application, and a Fast Ethernet application.

5. The method of claim 2 wherein the at least one control signal and the at least one status signal include a TX FAULT signal, a TX DISABLE signal, a RATE-SELECT signal, and a Loss of Signal (LOS) signal.

6. The method of claim 1 wherein the at least one of the TX CLOCK signal, the TX DATA signal, the RX CLOCK signal, and the RX DATA signal is arranged to pass

through a switching mechanism which is arranged to enable the plurality of single-ended pins to be in communication with a suitable logic module of the host device.

7. The method of claim 6 wherein the lower speed application is one of a T1/E1 application and a T3/E3 application, and the suitable logic module is one of a T1/E1 logic module and a T3/E3 logic module.

8. The method of claim 1 wherein determining when the SFP transceiver is suitable for use in supporting the lower speed application includes obtaining information from an ID ROM of the SFP transceiver.

9. The method of claim 1 wherein the lower speed application is one of a T1/E1 application and a T3/E3 application.

10. A method for providing a data path through a Small Form Factor Pluggable (SFP) transceiver, the SFP transceiver being substantially interfaced with a host device, the host device including a serializer-deserializer (SERDES) and a plurality of lines which substantially bypass the SERDES, the SFP transceiver including a plurality of pins which are arranged to interface with the plurality of lines which substantially bypass the SERDES, the method comprising:

determining when the SFP transceiver is arranged to be used to support lower speed applications; and

using the plurality of pins arranged to interface with the plurality of lines which substantially bypass the SERDES to provide at least one of a TX CLOCK signal, a TX DATA signal, an RX CLOCK signal, and an RX DATA signal when it is determined that the SFP transceiver is arranged to support the lower speed applications.

11. The method of claim 10 further including:

using the plurality of pins arranged to interface with the plurality of lines which substantially bypass the SERDES to provide at least one control signal and at least one status signal.

12. The method of claim 11 wherein when it is determined that the SFP transceiver is not arranged to support the lower speed applications, the SFP transceiver is being used for a higher speed application.

13. The method of claim 12 wherein the higher speed application is one of a Fiber Channel application, a Gigabit Ethernet application, and a Fast Ethernet application.

14. The method of claim 11 wherein the at least one control signal and the at least one status signal include a TX FAULT signal, a TX DISABLE signal, a RATE-SELECT signal, and a Loss of Signal (LOS) signal.

15. The method of claim 10 wherein the at least one of the TX CLOCK signal, the TX DATA signal, the RX CLOCK signal, and the RX DATA signal is arranged to pass through a switching mechanism which is arranged to enable the plurality of single-ended pins to be in communication with a suitable logic module of the host device.

16. The method of claim 15 wherein the lower speed application is one of a T1/E1 application and a T3/E3 application, and the suitable logic module is one of a T1/E1 logic module and a T3/E3 logic module.

17. The method of claim 10 wherein determining when the SFP transceiver is suitable for use in supporting the lower speed application includes obtaining information from an ID ROM of the SFP transceiver.

18. The method of claim 10 wherein the lower speed application is one of a T1/E1 application and a T3/E3 application.

19. A device suitable for use in a network, the device comprising:

a board, the board including a connector block, a serializer-deserializer (SERDES), and a plurality of lines which are coupled to the connector block and substantially bypass the SERDES;

a Small Form Factor Pluggable (SFP) transceiver, the SFP transceiver being arranged to interface with the connector block, the SFP transceiver including a plurality of pins arranged to interface with the plurality of lines which are coupled to the connector block and substantially bypass the SERDES;

code devices for determining when the SFP transceiver is suitable for use in supporting lower speed applications; and

code devices for using the plurality of pins to provide at least one of a TX CLOCK signal, a TX DATA signal, an RX CLOCK signal, and an RX DATA signal when it is determined that the SFP transceiver is arranged to support the lower speed applications.

20. The device of claim 19 wherein the plurality of pins is a plurality of single-ended pins, the device further including:

code devices for using the plurality of single-ended pins to provide at least one control signal and at least one status signal when it is determined that the SFP transceiver is not arranged to support the lower speed applications.

21. The device of claim 20 wherein when it is determined that the SFP transceiver is not arranged to support the lower speed applications, the SFP transceiver is being used for a higher speed application.

22. The device of claim 21 wherein the higher speed application is one of a Fiber Channel application, a Gigabit Ethernet application, and a Fast Ethernet application, and the lower speed application is one of a T1/E1 application and a T3/E3 application.

23. The device of claim 20 wherein the at least one control signal and the at least one status signal include a TX FAULT signal, a TX DISABLE signal, a RATE-SELECT signal, and a Loss of Signal (LOS) signal.

24. The device of claim 19 wherein the board includes a switching mechanism and a plurality of logic modules, the switching mechanism being in communication with the plurality of logic modules, and wherein the at least one of the TX CLOCK signal, the TX DATA signal, the RX CLOCK signal, and the RX DATA signal is arranged to pass through the switching to a suitable logic module of the plurality of logic modules.

25. The device of claim 24 wherein the lower speed application is one of a T1/E1 application and a T3/E3 application, and the suitable logic module is one of a T1/E1 logic module and a T3/E3 logic module.

26. The device of claim 19 wherein the code devices for determining when the SFP transceiver is suitable for use in supporting the lower speed application include code devices for obtaining information from an ID ROM of the SFP transceiver.

27. The device of claim 19 wherein the lower speed application is one of a T1/E1 application and a T3/E3 application.